WHAT IS CLAIMED IS:

1. A resistor comprising:

a semiconductor layer;

a body region formed in a portion of the semiconductor layer, the body region being doped to a first conductivity type and having a first resistivity;

a first contact region formed in the semiconductor layer adjacent the body region, the first contact region being doped to the first conductivity type;

a second contact region formed in the semiconductor layer spaced from the first contact region by the body region, the second contact region being doped to the first conductivity type;

a dielectric layer overlying the body region, said dielectric comprising a material with a relative permittivity greater than about 8; and

an electrode overlying said dielectric.

2. The resistor of claim 1 wherein the dielectric layer comprises a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof.

3. The resistor of claim 1 wherein the dielectric layer has a relative permittivity greater than about 10.

4. The resistor of claim 1 wherein the dielectric layer has a relative permittivity greater than about 20.

5. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than about 5 angstroms.

6. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than about 20 angstroms.

7. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than about 40 angstroms.

8. The resistor of claim 1 wherein the semiconductor layer comprises a silicon layer.

9. The resistor of claim 1 wherein the semiconductor comprises silicon and germanium.

10. The resistor of claim 1 wherein the semiconductor layer has a thickness in the range of about 20 angstroms to about 400 angstroms.

11. The resistor of claim 1 further comprising an insulator layer underlying the semiconductor layer.

12. The resistor of claim 11 wherein the insulator layer comprises silicon oxide.

13. The resistor of claim 1 wherein the electrode comprises a semiconductor.

14. The resistor of claim 1 wherein the electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

15. The resistor of claim 1 wherein the electrode comprises a metallic nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, and tantalum nitride, and combinations thereof.

16. The resistor of claim 1 wherein the electrode comprises a metallic silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, and erbium silicide, and combinations thereof.

17. The resistor of claim 1 wherein the electrode comprises a metallic oxide selected from the group consisting of ruthenium oxide, and indium tin oxide, and combinations thereof.

18. The resistor of claim 1 wherein the electrode has a width larger than about 0.1 microns.

19. The resistor of claim 1 wherein the electrode has a width larger than about 1 micron.

20. The resistor of claim 1 wherein the electrode has a length larger than about 0.1 microns.

21. The resistor of claim 1 wherein the electrode has a length larger than about 1 micron.

22. The resistor of claim 1 wherein the first conductivity type is n-type.

23. The resistor of claim 1 wherein the first conductivity type is p-type.

24. The resistor of claim 1 further comprising spacers formed on sides of the electrode.

25. The resistor of claim 24 wherein the spacers comprise silicon nitride.

1 26. The resistor of claim 24 further comprising an etch-stop layer overlying the electrode and
2 the spacers.

1 27. The resistor of claim 26 wherein the etch-stop layer comprise silicon nitride.

28. A silicon-on-insulator resistor comprising:

a silicon layer overlying an insulator layer;

a body region formed in a portion of the silicon layer;

a dielectric layer overlying the body region, said dielectric comprising a high permittivity dielectric layer;

a top electrode overlying said dielectric layer; and

a pair of doped regions formed in the silicon layer oppositely adjacent the body region, the pair of doped regions being doped to the same conductivity type as the body region.

29. The resistor of claim 28 wherein the high permittivity dielectric is selected from a group comprising of aluminum oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, and tantalum oxide, and combinations thereof.

30. The resistor of claim 28 wherein the permittivity dielectric layer comprises hafnium oxide.

31. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity greater than about 8.

32. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity greater than about 10.

33. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity greater than about 20.

1 34. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about
2 5 angstroms.

1 35. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about
2 20 angstroms.

1 36. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about
2 40 angstroms.

1 37. The resistor of claim 28 wherein the silicon layer is a strained silicon layer.

1 38. The resistor of claim 28 wherein the silicon layer has a thickness in the range of about 20
2 angstroms to about 1000 angstroms.

1 39. The resistor of claim 28 wherein the silicon layer has a thickness in the range of about 20
2 angstroms to about 400 angstroms.

1 40. The resistor of claim 28 wherein the insulator layer comprises silicon oxide.

1 41. The resistor of claim 28 wherein the electrode comprises polycrystalline silicon,
2 polycrystalline silicon-germanium, a metal, a metallic nitride, a metallic silicide, and a metallic
3 oxide, and combinations thereof.

1 42. The resistor of claim 41 wherein the metal is selected from the group consisting of
2 molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

1 43. The resistor of claim 41 wherein the metallic nitride is selected from the group consisting
2 of molybdenum nitride, tungsten nitride, titanium nitride, and tantalum nitride, and combinations
3 thereof.

1 44. The resistor of claim 41 wherein the metallic silicide is selected from the group
2 consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide,
3 platinum silicide, and erbium silicide, and combinations thereof.

1 45. The resistor of claim 28 wherein the electrode has a width greater than about 0.1 microns.

1 46. The resistor of claim 28 wherein the electrode has a width greater than about 1 micron.

1 47. The resistor of claim 28 wherein the electrode has a length greater than about 0.1
2 microns.

1 48. The resistor of claim 28 wherein the electrode has a length greater than about 1 micron.

1 49. The resistor of claim 28 wherein the body and the doped regions are doped n-type.

1 50. The resistor of claim 28 wherein the body and the doped regions are doped p-type.

1 51. The resistor of claim 28 further comprising spacers formed on sides of the electrode.

1 52. The resistor of claim 51 wherein the spacers comprise silicon nitride.

1 53. The resistor of claim 51 further comprising an etch-stop layer overlying the electrode and
2 the spacers.

54. The resistor of claim 53 wherein the etch-stop layer comprise silicon nitride.

55. The resistor of claim 54 further comprising an inter-layer dielectric overlying the etch-stop layer.

56. The resistor of claim 55 wherein the inter-layer dielectric comprises silicon oxide.

57. The resistor of claim 55 further comprising a contact plug formed through the inter-layer dielectric and in electrical contact with the resistor.

58. The resistor of claim 28 further comprising a shallow trench isolation region adjacent the silicon layer.

59. The resistor of claim 28 wherein the resistor is formed in an active area of the silicon layer and wherein the active area is isolated from other active areas that overlie the insulator layer by mesa isolation.

60. A method of forming a resistor, the method comprising:

providing a silicon-on-insulator substrate that includes a silicon layer overlying an insulator layer;

forming a resistor body of a first conductivity type in a portion of the silicon layer;

forming a dielectric layer overlying the body region, the dielectric layer comprising a material with a relative permittivity greater than about 8;

forming a top electrode on the dielectric layer; and

forming a pair of doped regions of the first conductivity type oppositely adjacent the body region.

61. The method of claim 60 wherein forming the resistor body comprises:

forming an active region;

forming isolation regions surrounding the active region; and

doping the active region.

62. The method of claim 61 wherein doping the active region employs an ion implantation with a dose in the range of about 10^{13} to about 10^{16} cm^{-2}.

63. The method of claim 60 wherein forming the dielectric layer comprises a chemical vapor deposition step.

64. The method of claim 60 wherein forming the dielectric layer comprises a sputtering deposition step.

65. The method of claim 60 wherein forming the dielectric layer comprises:

forming an interfacial oxide layer; and

forming a high permittivity dielectric layer.

66. The method of claim 60 wherein forming the pair of doped regions comprises:

doping a portion of the silicon layer not covered by the top electrode;

forming spacers on sidewalls of the top electrode; and

doping a portion of the silicon layer not covered by the top electrode and the spacers.

67. The method of claim 66 wherein the spacers comprise silicon nitride.

68. The method of claim 66 further comprising:

depositing an etch-stop layer over the top electrode and the spacers;

forming an inter-layer dielectric over the etch-stop layer;

forming contact holes in the inter-layer dielectric layer; and

filling the contact holes with a conductive material to form contact plugs.

69. The method of claim 68 wherein the etch-stop layer comprises silicon nitride.

70. The method of claim 68 wherein the inter-layer dielectric comprises silicon oxide.

71. The method of claim 68 wherein a first contact plug electrically contacts one of the pair of doped regions and a second contact plug electrically contacts the top electrode, said first and second contact plugs being electrically connected.

72. The method of claim 60 wherein the insulator layer comprises silicon oxide.

73. The method of claim 60 wherein the insulator layer has a thickness of less than about 1200 angstroms.

74. The method of claim 60 wherein the silicon layer has a thickness in the range of about 20 angstroms to about 1000 angstroms.

75. The method of claim 60 wherein the top electrode comprises a semiconductor.

76. The method of claim 60 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

77. The method of claim 60 wherein the top electrode comprises a metallic nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

78. The method of claim 60 wherein the top electrode comprises a metallic silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, and erbium silicide, and combinations thereof.

79. The method of claim 60 wherein the top electrode comprises a metallic oxide selected from the group comprising of ruthenium oxide, and indium tin oxide, and combinations thereof.

80. The method of claim 60 wherein the dielectric layer comprises a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, and zirconium silicate, and combinations thereof.

1 81. The method of claim 60 wherein the dielectric layer has a relative permittivity of larger
2 than about 10.

1 82. The method of claim 60 wherein the dielectric layer has a relative permittivity of larger
2 than about 20.

1 83. The method of claim 60 wherein the dielectric has a physical thickness greater than about
2 5 angstroms.

1 84. The method of claim 83 wherein the dielectric has a physical thickness greater than about
2 20 angstroms.

1 85. The method of claim 84 wherein the dielectric has a physical thickness greater than about
2 40 angstroms.

1 86. The method of claim 60 wherein the electrode has a width greater than about 0.1 microns.

1 87. The method of claim 60 wherein the electrode has a width greater than about 1 micron.

1 88. The method of claim 60 the electrode has a length greater than about 0.1 microns.

1 89. The method of claim 61 wherein the electrode has a length greater than about 1 micron.

90. A silicon-on-insulator device comprising:

an active area comprising a silicon layer overlying an insulator layer;

a body region of a first conductivity type formed in a portion of the silicon layer;

a dielectric layer overlying the body region, said dielectric comprising a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof;

a top electrode overlying the dielectric layer; and

a pair of doped regions of the first conductivity type formed in the silicon layer oppositely adjacent the body region.

91. The device of claim 90 wherein the dielectric layer comprises hafnium oxide.

92. The device of claim 90 wherein the silicon layer has a thickness in the range of about 20 angstroms to about 400 angstroms.

93. The device of claim 90 and further comprising a second active area overlying the insulator layer, the second active area including a transistor formed therein.

94. The device of claim 93 wherein the transistor includes a gate dielectric formed of the same material as the dielectric layer overlying the body region.

95. The device of claim 93 wherein the transistor includes a gate dielectric formed of a different material as the dielectric layer overlying the body region.

96. The device of claim 93 wherein the transistor includes a gate electrode formed of the same material as the top electrode.

97. The device of claim 90 and further comprising an interfacial layer overlying and abutting the body region, the dielectric layer overlying the interfacial layer.

98. The device of claim 97 wherein the interfacial layer comprises silicon oxide or silicon oxynitride.

99. A silicon-on-insulator device comprising:

a substrate;

an insulator layer overlying the substrate;

an active area formed in a silicon layer overlying the insulator layer;

a body region of a first conductivity type formed in a portion of the silicon layer;

an interfacial layer overlying and abutting the body region;

a high-k dielectric layer overlying the interfacial layer, the high-k dielectric layer comprising a material having a relative permittivity greater than about 8;

a top electrode overlying the high-k dielectric layer; and

a pair of doped regions of the first conductivity type formed in the active area oppositely adjacent the body region.

100. The device of claim 99 wherein the high-k dielectric comprises a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof.

101. The device of claim 100 wherein the dielectric layer comprises hafnium oxide.

102. The device of claim 100 and further comprising a second active area overlying the insulator layer, the second active area including a transistor formed therein.

103. The device of claim 102 wherein the transistor includes a gate dielectric comprising a material having a relative permittivity greater than about 8.

104. The device of claim 103 wherein the gate dielectric and the high-k dielectric comprise the same material.

105. The device of claim 102 wherein the transistor includes a gate electrode formed of the same material as the top electrode.

106. The device of claim 99 wherein the interfacial layer comprises silicon oxide.

107. The device of claim 99 wherein the interfacial layer comprises silicon oxynitride.

108. An electrostatic discharge protection circuit comprising:

an I/O pad;

a circuit that is to be protected;

a diode coupled between the I/O pad and a reference voltage node;

a resistor coupled between the I/O pad and the circuit, the resistor including a body region, a first contact region adjacent the body region to electrically couple the body region to the I/O pad, a second contact region adjacent the body region to electrically couple the body region to the circuit, a dielectric layer having a relative permittivity greater than about 8 overlying the body region, and an electrode overlying the dielectric layer.

109. The circuit of claim 108 wherein the diode comprises:

a diode body region;

a diode dielectric having a relative permittivity greater than about 8 overlying the diode body region;

a diode electrode overlying the diode dielectric; and

a p-doped region and an n-doped region oppositely adjacent to the diode body region.

110. The circuit of claim 109 wherein the p-doped region of the diode is electrically coupled to the I/O pad and the n-doped region of the diode is electrically coupled to the reference voltage node.

111. The circuit of claim 109 wherein the n-doped region of the diode is electrically coupled to the I/O pad and the p-doped region of the diode is electrically coupled to the reference voltage node.

112. The circuit of claim 108 and further comprising a second diode coupled between the I/O pad and a second reference voltage node.

113. The circuit of claim 112 wherein the second diode comprises:

a diode body region;

a diode dielectric having a relative permittivity greater than about 8 overlying the diode body region;

a diode electrode overlying the diode dielectric; and

a p-doped region and an n-doped region oppositely adjacent to the diode body region.

114. The circuit of claim 112 and further comprising:

a second circuit; and

a second resistor coupled between the second circuit and the I/O pad, the second resistor comprising a body region, a first contact region adjacent the body region to electrically couple

the body region to the I/O pad, a second contact region adjacent the body region to electrically couple the body region to the second circuit, a dielectric layer having a relative permittivity greater than about 8 overlying the body region, and an electrode overlying the dielectric layer.

115. The circuit of claim 114 wherein the circuit comprises an output circuit and wherein the second circuit comprises an input circuit.